

REMARKS

In the Office Action dated February 23, 2005, claims 1-25 were presented for examination. The Examiner objected to the Specification, and specifically, page 2, line 16. In addition, claims 1-25 were rejected under 35 U.S.C. §102(b).

Applicant wishes to thank the Examiner for the careful and thorough review and action on the merits in this application. The following remarks are provided in support of the pending claims and responsive to the Office Action of February 23, 2005 for the pending application.

I. Objection to the Disclosure

The Specification was objected to as containing an informality at page 2, line 16. The Applicant has amended the Specification with a corrected paragraph. Accordingly, Applicant respectfully requests the Examiner to enter the correction and to remove this objection.

II. Rejection of claims 1-25 under 35 U.S.C. §102(b)

Claims 1-25 were rejected under 35 U.S.C. §102(b) as being anticipated by *Robertson*, U.S. Patent No. 5,850,632. The *Robertson* patent '632 relates to a multiprocessor integrated circuit for image and graphics processing. More specifically, *Robertson* discloses a transfer controller in the circuit for mediating access to system memory. "Transfer controller 80 must handle many different types of requests from the processors. In order to assure optimal system performance, these requests are prioritized by their urgency and importance." Col. 13, lines 64-67. "Whenever transfer controller 80 receives multiple requests from different processors of the same priority, it will form a round robin between them . . . a fixed cyclical priority scheme." Col. 15, lines 37-40. However, *Robertson* does not disclose modifying a shared resource. Nor does *Robertson* force a write operation to non-local memory to precede the storage of a reference from an existing element of a shared resource to a new element of the shared resource, and allow a

write operation to local memory to execute in an arbitrary order, *i.e.* at any time prior to storing the pointer from the existing element of the shared resource to the new element of the shared resource. Rather, as noted by the Examiner, *Robertson* shows memory access cycles to determine replacement of prior cache entries. See Col. 31, lines 17-19. However, this is not equivalent to Applicant's invention. Applicant is not replacing cache entries. Rather, Applicant is setting the ordering of write operations with respect to a change in a shared resource. Accordingly, the ordering of memory operations of *Robertson* operate under different parameters and a different environment than that claimed by Applicant.


Applicant's invention applies to write operations to both local and non-local memory. There is no teaching in *Robertson* for allowing an arbitrary order of execution of write operations from local memory while requiring execution of write operations between local and non-local memory be executed prior to storing a pointer within a new element in a shared resource. In order for the claimed invention to be anticipated under 35 U.S.C. §102(b), the prior art must teach all claimed limitations presented by the claimed invention. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." MPEP §2131 (citing *Verdegaal Bros. v. Union Oil Co. of California*, 814 F. 2d 628, 631, 2 U.S.P.Q. 2d 1051, 1053 (Fed. Cir. 1987)). As mentioned above, *Robertson* does not show all of the elements as claimed by Applicant in pending claims 1-25, and specifically amended claims 1, 12, and 22. Specifically, *Robertson* does not support the element of forcing a write operation to non-local memory to precede storage of a reference from an existing element of a shared resource to a new element of the shared resource. Similarly, *Robertson* does not support the element of allowing a write operation to local memory to occur at any time prior to storage of a pointer from an existing element of the shared resource to a new element of the shared resource, as shown in Applicant's pending claims. Accordingly, *Robertson* clearly fails to teach the limitations pertaining to the arbitrary nature of execution of write operations in local memory in combination with explicit ordering of write operations to non-local memory as presented in Applicant's pending claims 1-25.

For the reasons outlined above, withdrawal of the rejection of record and an

allowance of this application are respectfully requested.

Respectfully submitted,

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